



**2010 Design and Verification Conference
Attendee Questionnaire Results
Based on 665 responses**

	Count	Percents
Which is your primary design language? (Pick one)		
Verilog	313	50%
VHDL	50	8%
C/C++	82	13%
SystemC	55	9%
SystemVerilog	127	20%
	627	100%
Which primary verification language do you currently use? (pick one)		
C/C++	89	14%
e	24	4%
OpenVera	18	3%
Verilog	156	25%
VHDL	26	4%
SystemC	53	9%
System Verilog	255	41%
	621	100%
Which primary verification language do you plan to use for your next design? (Pick one)		
C/C++	79	13%
e	18	3%
OpenVera	10	2%
Verilog	97	16%
VHDL	18	3%
SystemC	73	12%
SystemVerilog	325	52%
	620	100%
Which primary property specification (assertion-based verification) language do you use or plan to use?		
Verilog	166	28%
VHDL	46	8%
PSL	32	5%
SystemVerilog (SVA)	346	59%
	590	100%
What design area(s) are you focused on? (Check all that apply)		
Systems Design	199	11%
Standard ICs	62	3%
ASICs	285	16%
DSP Design	65	4%
Microprocessor/Microcontroller Design	100	6%
FPGAs & PLDs	192	11%
Multi-Chip Modules	45	3%
PCBs	43	2%
Library Development	33	2%
Analog/Mixed Signal	68	4%
EDA Tools	227	13%
Verification	297	17%
SOCs	162	9%
	1778	100%
What on-chip buses do you intend to use in the next 12 months?		
AMBA 2.0 AHB/APB	166	19%
AMBA 3 AXI	141	16%
OCP 2.0	38	4%
OCP 2.1	55	6%
CoreConnect	26	3%
Others/Proprietary	181	21%
None	263	30%
	870	100%

	Count	Percents
What standard interface do you expect to use in the next 12 months?		
PCI Express 1.1	57	5%
PCI Express 2.0	194	17%
USB 2.0/OTG	143	13%
Serial ATA	91	8%
10G Ethernet	94	8%
10/100/1G Ethernet	118	10%
Wireless USB	64	6%
PCI/PCI-X	75	7%
CE-ATA	13	1%
None	279	25%
	1128	100%
What is the size in gates of your current/last design? (Pick one)		
Not Applicable	235	37%
< 1M	62	10%
1 - 3M	62	10%
3 - 5M	31	5%
5 - 10M	69	11%
10M - 50M	98	15%
>50M	78	12%
	635	100%
How many clock domains do your designs average?		
1	24	4%
2	48	8%
2 - 5	167	26%
5 - 10	114	18%
10 - 20	47	7%
>20	39	6%
Not Applicable	193	31%
	632	100%
What is your number one design constraint?		
Low power	226	38%
Size/density	80	13%
Performance/throughput	293	49%
	599	100%
What are the two main reasons for your attendance at DVCon?		
Learn new techniques to improve your design process	235	18%
Learn new methodologies to improve your verification process	331	26%
Learn about new developments in design tools	226	18%
Meet and network with other engineers in the industry	301	24%
Learn about industry in general	187	15%
	1280	100%
Which category most closely describes your job description? (Pick one)		
Senior Management	107	17%
Engineering Management	116	18%
Design Engineer	111	17%
System Architecture	28	4%
Application Engineer	25	4%
Marketing & Sales	37	6%
Technical Marketing	21	3%
Product Marketing	17	3%
Sales	18	3%
Research/Academic	18	3%
CAD	27	4%
Verification Engineer	114	18%
	639	100%
DVCon provides an email list of attendees to exhibitors. If you DO NOT want to receive this correspondence check unsubscribe below.		
Unsubscribe	260	