2007 Design and Verification Conference Attendee Questionnaire Results (Based on 692 responses)

1) Which is your primary language?

Verilog	56%
VHDL	9%
C/C++	13%
SystemC	9%
SystemVerilog	13%

2 Which primary verification language do you use?

C/C+	18%
E	7%
OpenVera	4%
Verilog	28%
VHDL	7%
System C	13%
System Verilog	23%

3) Which primary verification language do you plan to use for your next design?

C/C++	16%
e	5%
OpenVera	1%
Verilog	16%
VHDL	4%
SystemC	15%
SystemVerilog	43%

4) Which primary property specification (assertion-based verification) language do you use?

Verilog	31%
VHDL	7%
PSL	12%
SystemVerilog (SVA)	49%

5) What design area(s) are you focused on? (Check all that apply)

Systems Design	12%
Standard ICs	4%
ASICs	19%
DSP Design	4%
Microprocessor/Microcontroller Design	5%
FPGAs & PLDs	9%
Multi-Chip Modules	2%
PCBs	2%
Library Development	2%
Analog/Mixed Signal	4%
EDA Tools	13%
Verification	15%
SOCs	9%

6) What on-chip buses do you intend to use in the next 12 months?

AMBA 2.0 AHB/APB	20%
AMBA 3 AXI	13%
OCP 2.0	6%
OCP 2.1	7%
CoreConnect	4%
Others/Proprietary	20%
None	30%

7) What interfaces standards do you expect to use in the next 12 months?

PCI Express 1.1	8%
PCI Express 2.0	15%
USB 2.0/OTG	12%
Serial ATA	9%
10G Ethernet	8%
10/100/1G Ethernet	11%
Wireless USB	6%
PCI/PCI-X	8%
CE-ATA	2%
None	21%

8) What is the size in gates of your current/last design?

Not applicable	
33%	
<1M	12%
1 – 3M	10%
3 – 5M	7%
5 – 10M	15%
10 – 50M	15%
>50M	8%

9) What are the two main reasons for your attendance at DVCon? (Check all that apply)

Learn new techniques to improve your design process	18%
Learn new methodologies to improve your verification process	26%
Learn about new developments in design tools	20%
Meet and network with other engineers in the Industry	21%
Learn about industry in general	15%

10) Which category most closely describes your job description?

Senior management	15%
Engineering management	17%
Design engineer	18%
System architecture	6%
Marketing & sales	13%
Research/academic	5%
CAD	7%
Verification engineer	19%