

Advance Registration Form

February 21-23, 2007

To register, mail or fax this form with payment to:

Design & Verification Conference & Exhibition
Attn: Registration Desk
5405 Spine Rd., Ste. 102
Boulder, CO 80301 USA



All registrations received after January 23, 2007, will be charged the "at-conference" rate. Payment with registration must be made in US dollars drawn from a US bank and made payable to: Design & Verification Conference & Exhibition. If payment is received from a non-US bank, attendees will be charged a collection fee of \$35.00. **TELEPHONE REGISTRATIONS WILL NOT BE ACCEPTED!** Fax registrations accepted with credit card payment only. **FAX Number: (303) 530-4334**

1 TYPE OR PRINT ATTENDEE INFORMATION

First Name _____ Last Name _____ Company _____
Address _____
City _____ State _____ Zip _____ Country _____
Phone _____ Fax _____ Email _____

2 CONFERENCE TUTORIALS – WEDNESDAY, FEBRUARY 21ST

(Please select any tutorial(s) you plan to attend. Wednesday Sponsored Tutorials are included in Full Conference Student and One-Day Only Registration. Includes access to one morning and one afternoon tutorial. Registrants will receive the (2) tutorial notes to their selected tutorials only. DVCon tutorial notes are not available for sale. Exhibit Only can purchase tutorials for \$50.00 per tutorial.

- _____ 1) (9:00 am - 12:30 pm): Pragmatic Plan-Driven Early Logic Design Verification from Formal to Coverage-Driven Simulation & Acceleration (Cadence)
- _____ 2) (9:00 am - 12:30 pm): Practical Applications of Mentor's Advanced Verification Methodology (AVM) (Mentor Graphics)

- _____ 3) (1:30 pm - 5:00 pm): Pragmatic Adoption of Verification Methodology Manual (VMM) for Re-usable Transaction-Based Testbenches in SystemVerilog (Synopsys)
- _____ 4) (1:30 pm - 5:00 pm): Using Formal Verification to Attain Completeness & Correctness (Denali, Jasper & Sun)
- _____ 5) (1:30 pm - 5:00 pm): SystemC Transaction Level Modeling Standards & Methodology Guidelines (SystemC)

3 REGISTRATION FEES

STATUS	Before Jan. 23, 2007	After Jan. 23, 2007
_____ Full Conference	\$455	\$550
_____ Student	\$250	\$250
_____ One-Day Only	\$275	\$325
_____ Exhibit-Only Pass circle day- _____ Thurs. _____ Fri.	FREE	FREE
_____ Exhibit-Only w/Wednesday Tutorials Morn. _____ Aft. _____	\$50/Tutorial	\$50/Tutorial
_____ Extra Hard Copy Proceedings	\$50	\$50

4 PAYMENT INFORMATION (required)

Registration Fees \$ _____	Credit Card: _____ VISA _____ MASTERCARD _____ AMERICAN EXP.
Proceedings \$ _____	Card # _____
Tutorial Fees \$ _____	Name _____ Exp. Date _____
TOTAL COST \$ _____	Please print name as it appears on the credit card

No refunds will be made unless a written request for cancellation is received prior to January 23, 2007. All refunds are subject to a \$25.00 processing fee. Requests for refunds received after the January 23, 2007 postmark date will not be honored and all registration fees will be forfeited. ***NO REGISTRATIONS WILL BE ACCEPTED POSTMARKED AFTER February 9, 2007, IN THE DVCON OFFICE.** After January 23, 2007, there will be at-conference registration only.

5 ATTENDEE SURVEY

1. Which is your primary design language? (Pick one)

- _____ 101) Verilog
- _____ 102) VHDL
- _____ 103) C/C++
- _____ 104) SystemC
- _____ 105) SystemVerilog
- _____ 106) Other _____

2. Which primary verification language do you use? (Pick one)

- _____ 201) C/C++
- _____ 202) e
- _____ 203) OpenVera
- _____ 204) Verilog
- _____ 205) VHDL
- _____ 206) SystemC
- _____ 207) SystemVerilog
- _____ 208) Other _____

3. Which primary verification language do you plan to use for your next design? (Pick one)

- _____ 301) C/C++
- _____ 302) e
- _____ 303) OpenVera
- _____ 304) Verilog
- _____ 305) VHDL
- _____ 306) SystemC
- _____ 307) SystemVerilog
- _____ 308) Other _____

4. Which primary property specification (assertion-based verification) language do you use?

- _____ 401) Verilog
- _____ 402) VHDL
- _____ 403) PSL
- _____ 404) System Verilog (SVA)
- _____ 405) Other _____

5. What design area(s) are you focused on? (Check all that apply)

- _____ 501) Systems Design
- _____ 502) Standard ICs
- _____ 503) ASICs
- _____ 504) DSP Design
- _____ 505) Microprocessor/Multicontroller Design
- _____ 506) FPGAs & PLDs
- _____ 507) Multichip Modules
- _____ 508) PCBs
- _____ 509) Library Development
- _____ 510) Analog/Mixed Signal
- _____ 511) EDA Tools
- _____ 512) Verification
- _____ 513) SoCs
- _____ 514) Other _____

6. What on-chip buses do you plan to use in the next 12 months?

- _____ 601) AMBA 2.0 AHB/APB
- _____ 602) AMBA 3 AXI
- _____ 603) OCP 2.0
- _____ 604) OCP 2.1
- _____ 605) CoreConnect
- _____ 606) Others/Proprietary _____
- _____ 607) None

7. What interface standards do you expect to use in the next 12 months?

- _____ 701) PCI Express 1.1
- _____ 702) PCI Express 2.0
- _____ 703) USB 2.0/OTG
- _____ 704) Serial ATA
- _____ 705) 10G Ethernet
- _____ 706) 10/100/1G Ethernet
- _____ 707) Wireless USB
- _____ 708) PCI/PCI-X
- _____ 709) CE-ATA
- _____ 710) None

8. What is the size in gates of your current/last design? (Pick one)

- _____ 801) Not Applicable
- _____ 802) <1M
- _____ 803) 1 - 3M
- _____ 804) 3 - 5M
- _____ 805) 5 - 10M
- _____ 806) 10 - 50M
- _____ 807) >50M

9. What are the two main reasons for your attendance at DVCon? (Check all that apply)

- _____ 901) Learn new techniques to improve your design process
- _____ 902) Learn new methodologies to improve your verification process
- _____ 903) Learn about new developments in design tools
- _____ 904) Meet and network with other engineers in the industry
- _____ 905) Learn about the industry in general

10. Which category most closely describes your job description? (Pick one)

- _____ 1001) Senior Management
- _____ 1002) Engineering Management
- _____ 1003) Design Engineer
- _____ 1004) System Architecture
- _____ 1005) Marketing & Sales
- _____ 1006) Research / Academic
- _____ 1007) CAD
- _____ 1008) Verification Engineer
- _____ 1009) Other _____

DVCon makes a list of attendees available to exhibitors. Check here if you do not want to be included on this list _____