

DVCon 2007 CALL FOR PAPERS

Conference on Using Hardware Design and
Verification Languages

February 21-23, 2007

DoubleTree Hotel, San Jose, California, USA

www.dvcon.org



DVCon is the premier conference on the usage of Hardware Description Languages (HDLs), and Hardware Verification Languages (HVLs) for the design and verification of electronic systems and integrated circuits. The focus of the conference is on specialized languages such as VHDL, PSL, Verilog, SystemVerilog, SystemC, e and VERA, as well as general purpose languages such as C and C++. Conference attendees are primarily designers of electronic systems, ASICs and FPGAs, as well as those involved in the research, development and application of Electronic Design Automation (EDA) tools. Presentations are highly technical in nature, and reflect real life experiences in using HDLs and HVLs.

We encourage you to contribute your experiences with using hardware design and verification languages and to participate in the valuable exchange of ideas.

TOPIC SUGGESTIONS

Any paper, tutorial or panel related to using HDLs, HVLs or other languages you have used for hardware design or verification will be considered. Here are a few topics that conference attendees might find useful:

- Experience using ESL and TLM for system-level design and verification
- Experiences with System-on-Chip design
- Designing and/or verifying complex ASICs and FPGAs
- Using multiple HDLs and/or HVLs in a design cycle
- Techniques for generating constrained-random test, or other automated stimulus generation methods
- Synthesizing transaction-level or abstract designs from high-level languages such as SystemC, System Verilog or C++, to RTL
- Experiences with hardware/software co-design and co-verification
- Experiences with mixed-signal simulation
- Verification techniques that really work (and what did not work)
- Verification methods that have achieved zero functional bugs in first silicon
- Assertion-based verification
- Coverage-driven verification
- Design and verification IP experiences, good and bad
- Measuring completeness and quality of verification: functional coverage, code coverage or other techniques
- Experience with formal technologies applied to verification, including the application of model checking and simulation together, or the use of dynamic formal verification tools
- Any topic involving the use of an HDL or HVL

CONFERENCE SCHEDULE:

Wednesday, February 21

- Half-day Tutorials am/pm
- Exhibition/pm

Thursday, February 22

- Opening Keynote Address
- Technical sessions
- Panel discussions
- Exhibition/pm

Friday, February 23

- Technical sessions
- Panel discussions

SUBMITTING A PROPOSAL

Proposals must be submitted on-line at www.dvcon.org.

Paper Proposals:

Proposal should be a short abstract of the paper, one to three paragraphs, 300 to 500 words maximum. The abstract must provide enough detail for the program committee to evaluate the technical depth and value of your paper. Be creative with your title!

Panel Proposals:

Proposal should be a short abstract of the panel topic, one to three paragraphs, 300 to 500 words maximum. The proposal should include the proposed panel members. Please provide enough detail for the program committee to evaluate the technical depth and value of your panel.

Special Session Proposals:

Special sessions may consist of embedded tutorials of one to two hours in length or focused on a specific topic with a list of invited papers/presentations relevant to that topic. Proposals for a special session must contain sufficient information to allow the Technical Program Committee (TPC) to assess the quality and interest of the proposal. Special session proposers will be expected to work closely with the TPC to shape and deliver a high-quality session.

Sponsored Tutorial Proposals:

A limited number of tutorials that are sponsored will be considered for inclusion in the program. Sponsored tutorials are free to conference registrants and provide an opportunity for an organization to reach an audience that is highly interested in a particular topic. If you are interested in proposing a sponsored tutorial, contact Kathy MacLennan at kathy@mpassociates.com. Sponsored tutorials will be considered on a first-come basis.

AUTHOR'S SCHEDULE:

- **September 19, 2006:** Paper and panel proposals due
- **October 5, 2006:** Tutorial proposals due
- **October 27, 2006:** Acceptance notification for all types
- **December 4, 2006:** Complete review draft of papers due
- **January 4, 2007:** Final paper due to proceedings printer

FINAL PUBLICATION REQUIREMENTS

If your proposed paper is accepted, an author kit with details on paper formatting will be sent to you. Final papers should be between four and eight pages, two-column, single-spaced. One author is required to present the paper at the DVCon Conference. A discounted registration fee of \$200 is offered to the presenter of the paper.

SPONSORED BY

The Design and Verification Conference, DVCon, is sponsored by Accellera, www.accelera.org. Accellera is an industry consortium dedicated to the development and standardization of design and verification languages.



For more information concerning the conference, please contact the conference management:

MP Associates, Inc.
5405 Spine Rd., Ste. 102
Boulder, CO 80301

Telephone: 303-530-4562 Fax: 303-530-4334

E-mail: kathy@mpassociates.com

